**Short CV July 2020**

**Ahmed Louri**

David and Marilyn Karlgaard Endowed Chair Professor

Director, High Performance Computer Architectures and Technologies Lab

Department of Electrical and Computer Engineering

George Washington University

Tel: (520) 331 2251, Email: louri@gwu.edu

**Education:**

Ph.D. 1988, University of Southern California, Los Angeles, California

**Distinctions and Awards:**

• Endowed Chair Professor of ECE, George Washington University, 2015

• IEEE Fellow, IEEE Computer Society

• Edward J. McCluskey Technical Achievement Award, IEEE Computer Society, 2020

• IEEE Outstanding Leadership Award, for the leadership to the field

• Outstanding Service Award, Computing and Communication Foundations (CCF), CISE Directorate, National Science Foundation, 2012

• Japan Society for the Promotion of Science (JSPS) Fellowship, Government of Japan, 1996, 2002, 2010

• Distinguished Researcher Fellowship, University of Paul Sabatier, Toulouse, France, 2002, 2003, 2009

• Centre National de Recherche Scientifique (CNRS) Fellowship, Government of France, 1995

• Advanced Telecommunications Organization of Japan Fellowship, Ministry of Post and Telecommunications, Government of Japan, 1994

• Best Journal Article of 1991 Award, IEEE MICRO, for presenting innovative optical solutions to fundamental problems in high-performance computing systems

• National Science Foundation Research Initiation Award (currently called NSF Career Award), 1989

• Teacher Appreciation Award, University of Arizona, 1991 – 1994

• Graduate Research Fellowship, Department of Electrical Engineering and Systems, University of Southern California, 1984 – 1988

• National Talent Search Scholarship, a five-year Award, Government of Algeria, 1983 – 1988

# Professional Service:

# I. Editorial Board

* **Editor-in-Chief,** *IEEE Transactions on Computers* (2019 - 2023)
* **Associate Editor,** *IEEE Transactions on Cloud Computing (2020 - present)*
* **Associate Editor,** *IEEE Transactions on Sustainable Computing* (2016 – present)
* **Associate Editor,** *Frontiers of Computer Science, Springer Publisher* (2019 – present)
* **Associate Editor,** *IEEE Transactions on Emerging Topics in Computing* (2015 –2019)
* **Associate Editor,** *IEEE Transactions on Computers* (2012 –2017)
* **Associate Editor,** *Cluster Computing:* *The Journal of Networks, Software Tools and Applications,* Baltzer Science Publishers (2000 – 2010)
* **Guest Editor** (with Avinash Kodi), *IEEE Transactions on Emerging Topics in Computing*(2016)
* **Guest Editor** (with Avinash Kodi),*Journal of Parallel and Distributed Computing*, Elsevier (2010)

# II. Other Significant IEEE Computer Society Committee Service

* **Chair**, Computer Society Fellows Committee, 2019.
* **Chair**, Editor-in-Chief Search Committee for the IEEE Transactions on Cloud Computing, 2019.
* **Vice-Chair,** IEEE Computer Society Fellow Committee (2013, 2017, and 2018).
* **Member** of the IEEE Computer Society Fellow Evaluation Committee (2012).
* **Member** of the IEEE Selection Committee for Editor-in-Chief, *IEEE Transactions on Sustainable Computing*, (2015).
* **Member** of the IEEE Computer Society Computer Entrepreneur Award Committee (2017).

**III. Conferences/Symposia/Workshops**

**Conference/Workshop Chair**

* **Area Chair**, The 34th IEEE International Parallel & Distributed Processing Symposium (IPDPS-2020), New Orleans, Louisiana, 2020
* **General Chair**, The 21st International Conference on High Performance Computing and Communications (HPCC-2019), Zhangjiajie, China, August 10 -12, 2019
* **General Chair**, The 25th IEEE Annual International Symposium on High Performance Computer Architecture (HPCA-25), Washington, D.C., February 15 - 20, 2019.
* **General Chair**, 2007 IEEE Annual International Symposium on High Performance Computer Architecture (HPCA-13), Phoenix, Arizona, February 10-14, 2007.
* **Publicity Chair**, 2000 IEEE International Symposium on High Performance Computer Architecture (HPCA-6), Toulouse, France, January 10-12, 2000.
* **General Co-Chair**, Second Workshop on Optics in Communications and Computer Sciences (WOCCS'99), Toulouse, France, March 10-12, 1999.
* **General Chair**, Workshop on Optics in High-Performance Computing Systems, (Workshop part of Euro-Par 1996), Lyon, France, August 27-29, 1996.
* **Group Lead**, DARPA Workshop on Future Directions for Interconnects, the University of Albany, SUNY, Albany, New York, May 21, 2013.

**Steering Committee Member (other than Technical Program Committee Member)**

* IEEE Transactions on Sustainable Computing, 2015 – present
* IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chips (MCSoCs), 2014 – present
* The International Symposium on High-Performance Computer Architecture (HPCA), 2007, 2008, 2009.
* The 11th ACS/IEEE International Conference on Computer Systems and Applications - AICCSA’13, Fez, Morocco, May 27- 30, 2013
* Founding and Steering Committee Member, NSF Workshop on Emerging Technologies for Interconnects (WETI), Washington, D.C., February 2 -3, 2012
* Founding and Steering Committee Member, NSF Workshop on Cross-Layer Power Optimization and Management, Los Angeles, California, February 10-11, 2012
* Euro-Par (Euro-Par is an annual series of international conferences held at the same time dedicated to the promotion and advancement of all aspects of parallel computing)

**Technical Program Committee Member**

* The 14th IEEE/ACM International Symposium on Networks-on-Chips (NOCS 2020), September 24 – 25, 2020 (Virtual Conference).
* The 26th International Symposium on High-Performance Computer Architecture (HPCA-26), San Diego, California, February 22 – 26, 2020
* The 37th IEEE International Conference on Computer Design, Abu Dhabi, United Arab Emirates, November 17 - 20, 2019
* The 13th IEEE/ACM International Symposium on Networks-on-Chips (NOCS 2019), New York, New York, October 17-18, 2019
* The 46th ACM/IEEE International Symposium on Computer Architecture (ISCA 2019), Phoenix, Arizona, June 22–26, 2019
* The 24th International Symposium on High-Performance Computer Architecture (HPCA-24), Vienna, Austria, February 24 – 28, 2018
* The 36th IEEE International Conference on Computer Design, Orlando, Florida, October 7 – 10, 2018
* The 12th IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip, Torino, Italy, October 4-5, 2018
* The 25th IEEE Symposium on High-Performance Interconnects, Santa Clara, California, 2017
* The 11th IEEE/ACM International Symposium on Networks-on-Chips (NOCS 2017), Seoul, South Korea, October 19-20, 2017
* The 22nd IEEE Symposium on High-Performance Computer Architecture (HPCA 2016), Barcelona, Spain, March 12 – 16, 2016
* The 43rd ACM/IEEE International Symposium on Computer Architecture (ISCA 2016), Seoul, South Korea, June 18 – 22, 2016
* The 9th IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Vancouver, Canada, September 28-30, 2015 and Nara, Japan, August 31 – September 2, 2016
* The 24th Annual Symposium on High-Performance Interconnects, Santa Clara, California, August 24 – 26, 2016
* The 20th International Symposium on High Performance Computer Architecture (HPCA), Orlando, Florida, February 14 – 19, 2014
* The International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XIV), Greece, July 14 -17, 2014
* The 7th ACM/IEEE International Symposium on Networks-on-Chip (NOCS), Tempe, Arizona, April 21 – 24, 2013
* The 22nd International Conference on Parallel Architectures and Compilation Techniques (PACT), Edinburgh, Scotland, September 7 – 11, 2013
* The 28th IEEE International Parallel & Distributed Processing Symposium, Phoenix, Arizona, May 19-23, 2014
* The 45th Annual IEEE/ACM International Symposium on Microarchitecture (Micro), Vancouver, Canada, December 1-5, 2012
* The 18th International Symposium on High-Performance Computer Architecture (HPCA), New Orleans, Louisiana, February 25 – 29, 2012
* The 6th ACM/IEEE International Symposium on Networks-on-Chip (NOCS), Copenhagen, Denmark, May 9 -11, 2012
* The 23rd International Symposium on Computer Architectures and High Performance Computing- SBAC-PAD 2011, Victoria, Brazil, October 26-29, 2011
* The 1st International Workshop on Hybrid Optical and Wireless Access Networks, Cannes, France, August 23-29, 2009
* The 4th ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS), San Jose, California, November 6 -7, 2008
* The 3rd ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS), Orlando, Florida, December 2 - 4, 2007
* The Annual International Symposium on High Performance Computing Systems & Applications, Canada, 2002-2004
* The 6th International Conference on Computer Science and Informatics, Durham, North Carolina, March 2002
* The IEEE International Workshop on Optics in Computer Science, San Francisco, California, April 2001
* The Workshop on Optics in Computer Science (WOCS'96), Metz, France
* The Workshop on Optics in Computer Science (WOCS'97) Geneva, Switzerland
* The Workshop on Optics in Computer Science (WOCS'98) Orlando, Florida
* The Workshop on Optics in Computer Science (WOCS'99) San Juan, Puerto Rico
* The IEEE Workshop on Optics in Computer Science (WOCS'2000) Cancun, Mexico
* The International Meeting on Components and Electronic Systems (IMCES'99), Sidi Bel Abbes, Algeria, May 17 - 18, 1999
* The Eleventh International Conference on Parallel and Distributed Computing and Systems (PDCS'99), Cambridge, Massachusetts, November 3-6, 1999
* The International Conference on Parallel Interconnects (PI'99), Anchorage, Alaska, October 17 - 19, 1999
* The International Symposium on Optical Science, Engineering, and Instrumentation, SPIE, Symposium in Algorithms, Devices, and Systems for Optical Information Processing II, Denver, Colorado, July 18-23, 1999
* Euro-Par'99, Toulouse, France, August 31-September 3, 1999
* The Fifth Symposium on Novel Machines Architectures (SympA'5), Rennes, France, June 8 - 11, 1999
* Optical Interconnects for High Performance Computing Workshop, Oak Ridge National Laboratory, October 1999
* The IEEE Annual International Phoenix Conference on Computers and Communications (IPCCC), March 1990-March 1996
* The International Conference on Massively Parallel Processing using Optical Interconnections (MPPOI'95), San Antonio, Texas
* The International Conference on Massively Parallel Processing using Optical Interconnections (MPPOI'96), Maui, Hawaii
* The International Conference on Massively Parallel Processing using Optical Interconnections (MPPOI'97), Montreal, Canada
* The International Conference on Massively Parallel Processing using Optical Interconnections (MPPOI'98), Las Vegas, Nevada
* The 9th Annual Workshop on Interconnections within High Speed Digital Systems, Santa Fe, New Mexico, May 17-20, 1998
* The OSA/IEEE International Topical Meeting on Optics in Computing (OC'98), Brugge, Belgium, June 17-20, 1998
* The 10th International Conference on Parallel and Distributed Computing and Systems (PDCS'98), Las Vegas, Nevada, October 28-31, 1998
* The International Symposium on Optical Science, Engineering, and Instrumentation, SPIE' 43rd Annual Meeting, San Diego, California, 19-24, July 1998
* The 8th International Conference on Computing and Information (ICCI'96), Ontario, Canada, June 1996
* The 1996 OSA/IEEE International Topical Meeting on Optics in Computing, Sandai, Japan, April 1996

**Publications:**

**I. Refereed Journal Articles**

1. Ke Wang, Hao Zheng, and Ahmed Louri, “TSA: Learning-Based Threat Detection and Mitigation for Secure System-On-Chip Architectures”, *IEEE Micro*, DOI: 10.1109/MM.2020.3003576, June 2020.
2. Hao Zheng and Ahmed Louri, “Agile: A Learning-enabled Power and performance-Efficient Network-on-Chip Design,” *IEEE Transactions on Emerging Topics in Computing (TETC)*, DOI: 10.1109/TETC.2020.3003496, June 2020.
3. Talha Canan, Savas Kaya, Avinash Karanth, Ahmed Louri, and Hao Xin, “Ultra-Compact and Low-Power Logic Circuits via Work-Function Engineering”, Submitted for publication, IEEE Transactions on VLSI, February 2019.
4. Ke Wang and Ahmed Louri, “CURE: High-Performance, Low-Power, Fault-Secure Network-on-Chip Architecture Using Reinforcement Learning,”, IEEE Transactions on Parallel and Distributed Computers (TPDS), DOI: 10.1109/TPDS.2020.2986297, April 2020.
5. Yuan Li and Ahmed Louri, “ALPHA: A Learning-Enabled High-Performance Network-on-Chip Router Design for Heterogeneous manycore Architectures, IEEE Transactions on Sustainable Computing, DOI: 10.1109/TSUSC.2020.2981340, March 2020.
6. Yuechen Chen and Ahmed Louri, “An Approximate Communication Framework for Networks-on-Chip,” , IEEE Transactions on Parallel and Distributed Computers (TPDS), vol. 31, issue 6, pp. 1434-1446, June 2020 .
7. T.F. Canan, S. Kaya, A. Karanth, and A. Louri, “Ultra-Compact and Low-Power Logic Circuits via Work-Function Engineering,” IEEE Journal of Exploratory Solid-State Computational Devices and Circuits, vol. 5, issue 2, pp. 94-102, December 2019.
8. Shanshan Liu, Ke Chen, Pedro Reviriego, Weiqiang Liu, Ahmed Louri and Fabrizio Lombardi, "Reduced Precision Redundancy for Error Tolerance and Reliable Processing of Data," IEEE Transactions on Emerging Topics in Computing (TETC), 10.1109/TETC.2019.2947617, December 2019.
9. D. Machovec, B. Khemka, N. Kumbhare, S. Pasrisha, A. Maciejewski, H.J. Siegel, A. Akoglu, G.A. Koenig, S. Hariri, C. Tunc, M. Wright, M. Hilton, R. Rambharos, C. Blandin, F. Fargo, A. Louri, N. Imam, “Utility-Based Resource Management in an Oversubscribed Energy- Constrained Heterogeneous Environment Executing Parallel Applications,” Journal of Parallel Computing, vol. 83, pp. 48-72, Apr. 2019.
10. Ahmed Louri, Jacques Collet, and Avinash Kodi, “Limit of Hardware Solutions for Self-Protecting Fault-Tolerant NoCs,” ACM Journal of Emerging Technologies for Computing, Vol. 15, Issue 1, February 2019
11. Quintin Fettes, Mark Clark, Razvan Bunescu, Avinash Kodi, and Ahmed Louri, “Dynamic Voltage and Frequency Scaling in NoCs with Supervised and Reinforcement Learning Techniques,” IEEE Transactions on Computers (TC), DOI: 10.1109/TC.2018.2875476, pp. 375 - 389, March 2019.
12. T.F. Canan, S. Kaya, A. Karanth, A. Louri, and H. Xin, “Ambipolar SB-FinFETs: A New Path to Ultra-Compact sub-10nm Logic Circuits,” IEEE Transactions on Electron Devices (TED), vol. 65, no. 12, 2018.
13. Avinash Karanth, Savas Kaya, Ashif Sikder, Daniel Carbaugh, Soumyasanta Laha, and Dominic DiTomaso, Ahmed Louri, , “Sustainability in Network-on-Chips by Exploring Heterogeneity in Emerging Technologies,” IEEE Transactions on Sustainable Computing, July 2018.
14. Hao Zheng and Ahmed Louri, “EZ-Pass: An Energy & Performance-Efficient Power-gating Router Architecture for Scalable NoCs,” IEEE Computer Architecture Letters (CAL), vol. 17, no. 1, pp. 88-91, Jan. 2018.
15. Dominic DiTomoso, Avinash Kodi, and Ahmed Louri, “Power-gating Techniques Applicable to Channel Buffers and Router Microarchitecture in NoCs,” submitted for publication, IEEE Transactions on Computer-Aided Design of Integrated Circuits & Systems (TCAD), June 2017.
16. J. Wu, A. Kodi, S. Kaya, A. Louri, and H. Xin, “Monopoles Loaded with 3D-Printed Dielectrics for Future Wireless Intra-Chip Communications,” IEEE Transactions on Antennas and Propagation, Vol. 65 No. 12, December 2017.
17. Pavan Poluri and Ahmed Louri, “Shield: A Reliable Network-on-Chip Router Architecture for Chip Multiprocessors,” IEEE Transactions on Parallel and distributed Computers (TPDS), Vol. 27, No. 10, pp. 3058-3070, October 2016.
18. Wo-Tak Wu and Ahmed Louri, “A Methodology for Cognitive NoC Design,” IEEE Computer Architecture Letters (CAL), Vol.15, Issue 1, Jan.-June 1, 2016.
19. Dominic DiTomaso, Avinash Kodi, Ahmed Louri and Razvan Bunescu, “Resilient and Power- Efficient Multi-Function Channel Buffers in Network-on-Chip Architectures,” IEEE Transactions on Computers, Vol. 64, No. 12, pp. 3555-3568, December 2015.
20. Tzyy-Juin Kao and Ahmed Louri, “Optical Multi-Level Signaling for High Bandwidth and Power- efficient On-Chip Interconnects,” IEEE Photonics Technology Letters, Vol. 27, No. 19, pp. 2051- 2054, October 2015.
21. Pavan Poluri and Ahmed Louri, “A Soft Error Tolerant Network-on-Chip Router Pipeline for Multi-core Systems,” IEEE Computer Architecture Letters (CAL), Vol. 14, No. 2, pp. 107 – 110, July- December, 2015.
22. Randy Morris, Avinash Kodi, Ahmed Louri and Ralph Whaley, “3D Stacked Nanophotonic Architecture with Minimal Reconfiguration,” IEEE Transactions on Computers, Vol. 63, No. 1, pp. 243-255, January 2014.
23. J. Sun, R. Lysecky, K. Shankar, A. Kodi, A. Louri and J. Wang, “Workload Assignment Considering NBTI Degradation in Multi-core Systems,” ACM Journal on Emerging Technologies in Computing Systems (JETC), Vol. 10, No. 1, pp. 1-22, January 2014.
24. D. DiTomaso, R. Morris, A. Kodi, A. Sarathy and A. Louri, “Extending the Energy-Efficiency and Performance with Channel Buffers, Crossbars and Topology Analysis for NoCs,” IEEE Transactions on VLSI (TVLSI), Vol. 21, No. 11, pp. 2141-2154, November 2013.
25. Ahmed Louri and Avinash Karanth Kodi, “Introduction to the Special Issue on Network-on-Chips (NoCs),” Journal of Parallel and Distributed Computing, Vol. 71, No. 5, pp. 623-624, May 2011.
26. Avinash Karanth Kodi and Ahmed Louri, “Energy-Efficient Bandwidth-Reconfigurable Photonic Networks for High-Performance Computing (HPC) Systems,” IEEE Journal of Selected Topics in Quantum Electronics, Special Issue on Green Photonics, Vol. 17, No. 2, pp. 384-395, March/April 2011.
27. Avinash Karanth Kodi and Ahmed Louri, “Multi-Dimensional and Reconfigurable Optical Interconnects for High-Performance Computing (HPC) Systems," IEEE Journal of Lightwave Technology, Vol. 27, No. 21, pp. 4634-4641, November 2009.
28. Avinash Karanth Kodi and Ahmed Louri, “Reconfigurable and Adaptive Photonic Networks for High-Performance Computing (HPC) Systems,” Applied Optics, special issue on Optical High- Performance Computing, Vol. 48, No. 22, pp. E13-E23, August 2009.
29. Avinash Karanth Kodi and Ahmed Louri, “OPTISIM: A System Simulation Methodology for Optically Interconnected High-Performance Computing Systems,” IEEE Micro, Vol. 28, No. 5, pp. 22-36, September/October 2008.
30. Avinash Karanth Kodi, Ashwini Sarathy and Ahmed Louri, “Adaptive Channel Buffers in On-Chip Interconnection Networks: A Power and Performance Analysis,” IEEE Transactions on Computers, Vol. 57, No. 9, pp. 1169 - 1182, September 2008.
31. Ashwini Sarathy, Avinash Karanth Kodi and Ahmed Louri, “Low Power, Low Area Network-on- Chip Architecture using Adaptive Channel Buffers,” IEEE Electronics Letters, Vol. 44, No. 8, pp. 512-513, April 10, 2008.
32. Avinash Kodi and Ahmed Louri, “A System Simulation Methodology of Optical Interconnects for High-Performance Computing (HPC) Systems,” OSA Journal of Optical Networking (JON), Vol. 6, No. 12, pp. 1282-1300, December 2007.
33. Chander Kochar, Avinash Kodi and Ahmed Louri, “Proposed Low-Power High-Speed Microring Resonator-based Switching Technique for Dynamically Reconfigurable Optical Interconnects,” IEEE Photonics Technology Letters, Vol. 19, No. 17, pp. 1304-1306, September 2007.
34. Chander Kochar, Avinash Karanth Kodi, and Ahmed Louri, “nD-RAPID: A Multi-Dimension Scalable Fault-tolerant Opto-Electronic Interconnection for Scalable High-Performance Computing Systems,” Journal of Optical Networking, special issue on Photonics in Switching, Vol. 6, No. 5, pp. 465-481, May 2007.
35. Avinash Karanth Kodi and Ahmed Louri, “RAPID for High-Performance Computing: Architecture and Performance Evaluation,” Applied Optics, Special Issue on Information Photonics, Vol. 45, No. 25, pp. 6326-6334, September 2006.
36. Avinash Karanth Kodi and Ahmed Louri, “Design of a High-Speed Optical Interconnect for Scalable Shared Memory Multiprocessors,” IEEE Micro, Special Issue Hot Interconnects 12, Vol. 25, No. 1, pp. 41-49, January/February 2005.
37. Ahmed Louri and Avinash Karanth Kodi, “An Optical Interconnection Network and a Modified Snooping Protocol for the Design of Large Scale Symmetric Multiprocessors (SMPs),” IEEE Transactions on Parallel and Distributed Systems, Vol. 15, No. 12, pp. 1093-1104, December 2004.
38. Avinash Karanth Kodi and Ahmed Louri, “RAPID: Reconfigurable and scalable All-Photonic Interconnect for Distributed shared memory multiprocessors,” IEEE/OSA Journal of Lightwave Technology, special issue on Optical Interconnects, Vol. 22, No. 9, pp. 2101-2110, September 2004.
39. Ahmed Louri and Avinash Karanth Kodi, “SYMNET: An Optical Interconnection Network for Large-scale, High-Performance Symmetric Multiprocessors,” Applied Optics, Vol. 42, No. 17, pp. 3407-3417, June 10, 2003.
40. Ahmed Louri and Avinash Karanth Kodi, “Parallel Optical Interconnection for Address Transactions in Large-scale, Cache-coherent Symmetric Multiprocessors,” IEEE Journal of Selected Topics in Quantum Electronics, special issue on Optical Interconnects, Vol. 9, No. 2, pp. 667-676, March/April, 2003.
41. Ahmed Louri and Avinash Karanth Kodi, “Scalable Optical Interconnection Networks for Symmetric Multiprocessors," Optics In Information Systems, Vol. 14, No. 1, March 2003.
42. Peng Yin Choo and Ahmed Louri, “Multi-wavelength Optical Processor for High-speed Parallel Relational Database Processing,” Asian Journal of Physics, special issue on Optical Information Technology, Vol. 10, No. 2 , pp. 169 - 185, July - September 2001.
43. Peng Yin Choo and Ahmed Louri, “Guidedwave Multiwavelength Polarization-insensitive Processing Module for Parallel Multicomparand Perfect-match Algorithm,” Optics Letters, Vol. 25, No. 20, pp. 1541 -1543, October 15, 2000.
44. Brian Webb and Ahmed Louri, “A Class of Highly Scalable Optical Crossbar-Connected Interconnection Networks For Parallel Computing Systems,” IEEE Transactions on Parallel and Distributed Systems, Vol. 11, No. 5, pp. 444 - 458, May 2000.
45. Daniel Litaize, Jacques Collet and Ahmed Louri, “Le Role de L'Optique dans les Ordinateurs,” Technique et Science Informatiques, January 2000.
46. Abram Detofsky, Peng Yin Choo and Ahmed Louri, “Towards a Monolithic Equivalency Processing Parallel Photonic Integrated Circuit (EP3IC),” Applied Optics, special issue on Optics in Computing, Vol. 39, No. 5, pp. 818 - 826, February 10, 2000.
47. J.H. Collet, D. Litaize, J. V. Campenhut, M. Desmulliez, A. Louri, H. Thienpont, C. Jesshope, J. Goodman, and Z. Vranesic, “Architectural Approaches to the Role of Optics in Mono and Multiprocessor Machines,” Applied Optics, special issue on Optics in Computing, Vol. 39, No. 5, pp. 671 - 682, February 10, 2000.
48. Peng Yin Choo, Abram Detofsky and Ahmed Louri, “A Multi-Wavelength Optical Content- Addressable Parallel Processor for High-Speed Parallel Relational Database Processing,” Applied Optics, Vol. 38, No. 26, pp. 5594 - 5604, September 10, 1999.
49. Brian Webb and Ahmed Louri, “An All-Optical Crossbar Switch using Wavelength Division Multiplexing and Vertical Cavity Surface Emitting Lasers,” Applied Optics, Vol. 38, No. 29, October 10, 1999.
50. Peng Yin Choo, Abram Detofsky and Ahmed Louri, “Optical Implementation of a Multi- Comparand Bit-Parallel Magnitude Comparison Algorithm using Wavelength and Polarization- Division Multiplexing with Application to Parallel Database Processing,” Optics Letters, Vol. 23, No. 17, pp. 1372 - 1375, September 1, 1998.
51. Ahmed Louri, Brent Weech, and Costas Neocleous, “A Spanning Multichannel Linked Hyper- cube: A Gradually Scalable Optical Interconnection Network for Massively Parallel Computing,” IEEE Transactions on Parallel and Distributed Systems, Vol. 9, No. 5, pp. 497 - 512, May 1998.
52. Ahmed Louri and C. Neocleous, “Incrementally Scalable Optical Interconnection Network with a Constant Degree and Constant Diameter for Parallel Computing,” Applied Optics, Vol. 36, No. 26, pp. 6594 - 6604, September 10, 1997.
53. Ahmed Louri and C. Neocleous, “A Spanning Bus Connected Hypercube: A New Scalable Optical Interconnection Network for Multiprocessors and Massively Parallel Systems,” IEEE/OSA Journal of Lightwave Technology, Vol. 15, No. 7, pp. 1241 - 1252, July 1997.
54. Ahmed Louri and Rajdeep Gupta, “Hierarchical Optical Ring Interconnection (HORN): Scalable Interconnection Network for Multiprocessors and Multicomputers,” Applied Optics, Vol. 36, No. 2, pp. 430 - 442, January 10, 1997.
55. Ahmed Louri, Stephen Furlonge, and Costas Neocleous, “Experimental Demonstration of the Optical Multi-Mesh Hypercube: Scalable Interconnection Network for Multiprocessors and Multicomputers,” Applied Optics, Vol. 35, No. 35, pp. 6909 - 6920, December 10, 1996.
56. Ahmed Louri and Stephen Furlonge, “Feasibility Study of a Scalable Optical Interconnection Network for Massively Parallel Processing Systems,” Applied Optics, Vol. 35, No. 8, pp. 1296 - 1308, March 10, 1996.
57. Ahmed Louri and Hongki Sung, “Optical Binary de Bruijn Networks for Massively Parallel Computing: Design Methodology and Feasibility Study,” Applied Optics, Vol. 34, No. 29, pp. 6714- 6723, October 10, 1995.
58. Ahmed Louri and Jongwhoa Na, “Design of an Optical Content-Addressable Parallel Processor for Expert Systems,” Applied Optics, Vol. 34, No. 23, pp. 5053 - 5064, August 10, 1995.
59. Ahmed Louri and Michael Major, “A Generalized Methodology for Modeling and Simulating Three-Dimensional Optical Interconnects using Diffraction Analysis,” Applied Optics, Vol. 34, No. 20, pp. 4052 - 4065, July 10, 1995.
60. Ahmed Louri, James Hatch Jr. and Jongwhoa Na, “A Novel Constant-Time Parallel Sorting Algorithm and its Optical Implementation Using Smart Pixels,” Applied Optics, Vol. 34, No. 17, pp. 3087 - 3097, June 10, 1995.
61. Ahmed Louri, James Hatch Jr. and Jongwhoa Na, “A Constant-Time Parallel Sorting Algorithm and its Optical Implementation,” IEEE MICRO, Chips, Systems, Software, and Applications, special feature article on Optical Processing and Computing, Vol. 15, No. 3, pp. 60 - 71, June 1995.
62. Ahmed Louri and James Hatch Jr., “An Optical Content-Addressable Parallel Processor for High- Speed Database Processing,” Applied Optics, Vol. 33, No. 35, pp. 8153 - 8164, December 10, 1994.
63. Ahmed Louri and James Hatch Jr., “An Optical Associative Parallel Processor for High-Speed Database Processing: Theoretical Concepts and Experimental Results,” IEEE Computer, IEEE Computer Society, special issue on Associative Processors, Vol. 27, No. 11, pp. 65 - 72, November 1994.
64. Ahmed Louri and Hongki Sung, “A Scalable Optical Hypercube-Based Interconnection Network for Massively Parallel Computing,” Applied Optics, Vol. 33, No. 32, pp. 7588 - 7599, November 10, 1994.
65. Ahmed Louri and Hongki Sung, “Three-Dimensional Optical Interconnects for High-Density Chip- to-chip and Board-to-board Communications,” IEEE Computer, IEEE Computer Society, Vol. 27, No. 10, pp. 27 - 37, October 1994.
66. Ahmed Louri and Hongki Sung, “An Optical Multi-Mesh Hypercube: A Scalable Optical Interconnection Network for Massively Parallel Computing,” IEEE/OSA Journal of Lightwave Technology, Vol. 12, No. 4, pp. 704 - 716, April 1994.
67. Ahmed Louri and Jongwhoa Na, “A Modeling and Simulation Methodology for Digital Optical Computing Systems,” Applied Optics, special issue on Optical Computing, Vol. 33, No. 8, pp. 1549- 1559, March 10, 1994.
68. Ahmed Louri and Hongki Sung, “An Efficient Implementation Methodology for Three- Dimensional Space-Invariant Hypercube-Based Free-Space Optical Interconnection Networks,” Applied Optics, Vol. 32, No. 35, pp. 7200-7209, December 10, 1993.
69. Ahmed Louri and Hongki Sung, “A Design Methodology for Three-Dimensional Space-Invariant Hypercube Networks Using Graph Bipartitioning,” Optics Letters, Vol. 18, No. 23, pp. 2050 - 2052, December 1, 1993.
70. Bernard P. Zeigler and Ahmed Louri, “A Simulation Environment for Intelligent Machine Architectures,” Journal of Parallel and Distributed Computing, special issue on Architectures and Tools for Artificial Intelligence, Vol. 18, pp. 77 - 88, July 1993.
71. Ahmed Louri and James Hatch, “Optical Implementation of a Single-Iteration Thresholding Algorithm with Applications to Parallel Database/Knowledge-Base Processing,” Optics Letters, Vol. 18, No. 12, pp. 992- 994, June 15, 1993.
72. Ahmed Louri and Jongwhoa Na, “Parallel Optical Rule-Based System for Fast Execution of Expert Systems,” Applied Optics, Vol. 32, No. 11, pp. 1863 - 1875, April 1993.
73. Ahmed Louri and Arthur Post, “A Complexity Analysis of Optical Computing Paradigms,” Applied Optics, special issue on Optical Computing, Vol. 31, No. 26, pp. 5568 - 5584, September 10, 1992.
74. Ahmed Louri, “An Optical Content-Addressable Parallel Processor: Architecture, Algorithms, and Design Concepts,” Applied Optics, Vol. 31, No. 17, pp. 3241 - 3258, June 10, 1992.
75. Ahmed Louri, “Three-Dimensional Optical Architecture and Data-Parallel Algorithms for Massively Parallel Computing,” IEEE MICRO, Vol. 11, No. 2, pp. 24 - 27, and pp. 65-82, April 1991. (Best Journal Article Award).
76. Ahmed Louri, “Parallel Implementation of Optical Symbolic Substitution Logic Using Shadow- Casting and Polarization,” Applied Optics, Vol. 30, No. 5, pp. 540 - 548, February 10, 1991.
77. Ahmed Louri, “Throughput Enhancement of Digital Optical Computing Systems,” Applied Optics, Vol. 29, No. 20, pp. 2979 - 2987, July 1990.
78. Ahmed Louri, “An Efficient Optical Implementation Method for Symbolic Substitution Logic Using Shadow-Casting,” Applied Optics, Vol. 28, No. 16, pp. 3264 - 3268, August 15, 1989.
79. Ahmed Louri, “A Parallel Architecture and Algorithms for Optical Computing,” Optics Communications, Vol. 72, pp. 27-36, July 1989.
80. Kai Hwang and Ahmed Louri, “Optical Multiplication and Division using Signed-Digit Symbolic Substitution,” Optical Engineering, special issue on Optical Computing, Vol. 28, No. 4, pp. 364 - 373, April 1989.

## II. Refereed Conference Papers

1. Yuechen Chen, and Ahmed Louri, “A Learning-based Accuracy Management for Approximate Communication in Multi-core Systems”, to appear in Proceedings of International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Hamburg, Germany, September 20-25, 2020.
2. Quintin Fettes, Kyle Shiflett, Avinash Karanth, Razvan Bunescu and Ahmed Louri, “Hardware–based Thread Migration to Reduce On-Chip Data Movement with Reinforcement Learning,” to appear in Proceedings of International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), Hamburg, Germany, September 20-25, 2020.
3. Kyle Shiflett, Avinash Karanth, Ahmed Louri and Razvan Bunescu, “Energy-Efficient Multiply-and-Accumulate Using Silicon Photonics for Deep Neural Networks,” to appear in proceedings of 2020 IEEE Photonics Conference (IPC), Vancouver, Canada, 27 September - 1 October 2020.
4. Hao Zheng, Ke Wang, and Ahmed Louri, “A Versatile and Flexible Chiplet-based System Design for Heterogeneous Manycore Architectures,” in proceedings of 57th Design Automation Conference (DAC’20), San Francisco, July 19-23, 2020.
5. Mark Clark, Yingping Chen, Avinash Karanth, Brian Ma, and Ahmed Louri, "DoZZNoC: Reducing Static and Dynamic Energy in NoCs with Low-Latency Voltage Regulators using Machine Learning," in Proceedings of 26th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2020), New Orleans, LA, May 18-22, 2020.
6. Kyle Shiflett , Dylan Wright, Avinash Karanth, and Ahmed Louri, " PIXEL: Photonic Neural Network Accelerator," in Proceedings of 34th IEEE International Symposium on High-Performance Computer Architecture (HPCA), San Diego, CA, February 22-26, 2020.
7. Yuechen Chen and Ahmed Louri, “An Online Quality Management Framework for Approximate Communication in Network-on-Chips,” in Proceedings of the 33rd International Conference on Supercomputing (ICS-2019), Phoenix, Arizona, June 26-28, 2019.
8. Ke Wang, Ahmed Louri, Avinash Karanth and Razvan Bunescu, “IntelliNoC: A Holistic Framework for Energy-Efficient and Reliable On-chip Communication for Manycores,” in Proceedings of the 46th International Symposium on Computer Architecture (ISCA-46), Phoenix, Arizona, June 22-26, 2019.
9. Hao Zheng and Ahmed Louri, “An Energy-Efficient Network-on-Chip Design using Reinforcement Learning,” in Proceedings of 56th Design Automation Conference (DAC’19), Las Vegas, NV, June 2-6, 2019.
10. Ke Wang, Ahmed Louri, Avinash Karanth and Razvan Bunescu, “Reinforcement Learning for Fault-tolerant, Energy-efficient NoC Design,” in Proceedings of Design and Test in Europe (DATE’19), Florence, Italy, March 25-29, 2019.
11. T. F. Canan, S. Kaya, A. Kodi, H. Xin and A. Louri, “10T and 8T Full Adders Based on Ambipolar XOR Gates with SB-FinFETs,” in Proceedings of 25th IEEE International Conference on Electronic Circuits and Systems (ICECS), Bordeaux, France, December 9-12, 2018.
12. Yuechen Chen, Md Farhadur Reza and Ahmed Louri, “DEC-NoC: An approximate Framework based on Dynamic Error Control with Applications to Energy-efficient NoCs,” in Proceedings of 36th IEEE International Conference on Computer Design (ICCD), Orlando, FL, October 7-10, 2018.
13. Y. Kelestemur, S. Laha, S. Kaya, A. Kodi, H. Xin, and A. Louri, “Sub-THz Tunable Push-Push Oscillators with FinFETs for Wireless NoCs,” in Proceedings of 61st IEEE International Midwest Symposium on Circuits and Systems, Windsor, Canada, August 5 – 8, 2018.
14. Mark Clark, Avinash Kodi, Razvan Bunescu and Ahmed Louri, “LEAD: Learning-enabled Energy-Aware Dynamic Voltage/Frequency Scaling in NoCs,” in Proceedings of 55th Design Automation Conference (DAC’18), San Francisco, CA, June 24-28, 2018.
15. Avinash Kodi, Kyle Shiflett, Savas Kaya and Soumyasanta Laha and Ahmed Louri, "Scalable Power-Efficient Kilo-Core Photonic-Wireless NoC Architectures," in Proceedings of 32nd IEEE International Symposium on Parallel and Distributed Processing (IPDPS), Vancouver, British Columbia, Canada, May 21 - 25, 2018.
16. Scott Van Winkle, Avinash Kodi, Razvan Bunescu, and Ahmed Louri, " Extending the Power-Efficiency and Performance of Photonic Interconnects for Heterogeneous Multicores with Machine Learning,", in Proceedings of 24th IEEE International Symposium on High-Performance Computer Architecture (HPCA), Vienna, Austria, February 24-28, 2018.
17. Priyankar Roychowdhury and Ahmed Louri, “Reconfigurable All-Photonic Inter-Rack Interconnect for Datacenters,” in Proceedings, Frontiers in Optics 2017, OSA Technical Digest, Optical Society of America, Washington, D.C., September 18 – 21, 2017.
18. T. F. Canan, S. Kaya, A. Kodi, H. Xin, and A. Louri, “Ultra-Compact sub-10nm Logic Circuits Based on Ambipolar SB-FinFETs,” in Proceedings, IEEE 60th International Midwest Symposium on Circuits and Systems, Boston, Massachusetts, August 6 – 9, 2017.
19. Y. Kelestemur, S. Laha, S. Kaya, A. Kodi, H. Xin, and A. Louri, "mm-wave Tunable Copitts Oscillators Based on FinFETS,” in Proceedings, IEEE Wireless and Microwave Technology Conference (WAMICON), Cocoa Beach, Florida, April 24 -25, 2017.
20. Dominic DiTomaso, Ashif Sikder, Avinash Kodi, and Ahmed Louri, “Machine Learning Enabled Power-Aware Network-on-Chip Design,” in Proceedings, Design Automation and Test in Europe, DATE’17, Lausanne, Switzerland, March 27 – 31, 2017.
21. Dominic DiTomaso, Travis Boraten, Avinash Kodi and Ahmed Louri, “Predicting and Mitigating Faults in NoCs using Machine Learning,” in Proceedings, IEEE/ACM International Conference on Microarchitecture (MICRO-49), Taipei, Taiwan, October 15- 19, 2016.
22. Ashif Sikder, Avinash Kodi and Ahmed Louri, “R-OWN: Reconfigurable Optical Wireless NoC Architectures,” in Proceedings, Third ACM International Conference on Nanoscale Computing and Communication (NanoCom), New York, New York, September 28-29, 2016.
23. Tzyy-Juin Kao and Ahmed Louri, “Design of High Bandwidth Photonic Network-on-Chip Architectures Using Optical Multilevel Signaling,” in Proceedings, 10th IEEE/ACM International Symposium on Networks-on-Chip (NOCS 2016), Nara, Japan, August 31 – September 2, 2016.
24. A. Kodi, A. Sikdar, A. Louri, S. Kaya and M. Kennedy, “OWN: Optical and Wireless Network-on-Chips (NoCs) for Kilo-core Architectures,” in Proceedings, the 23rd Annual Symposium on High-Performance Interconnects (2015 IEEE Hot Interconnects), Santa Clara, California, August 26-28, 2015.
25. B. Khemka, D. Machovec, C. Blandin, H.J. Siegel, S. Hariri, A. Louri, C. Tunc, F. Fargo and A.A. Maciejewski, “Resource Management in Heterogeneous Parallel Computing Environments with Soft and Hard Deadlines,” in Proceedings, 11th edition of the Metaheuristics International Conference (MIC 2015), Agadir, Morocco, June 7-10, 2015.
26. S. Zuckerman, H. Wei, H. Wong, G.R. Gao, J-L. Gaudiot and A. Louri, “A Holistic Dataflow-Inspired System Design,” in Proceedings, Fourth Workshop on Data- Flow Execution Models for Extreme Scale Computing (DFM 2014), held conjunction with Parallel Architectures and Compilation Techniques (PACT), Edmonton, Alberta, Canada, August 24, 2014.
27. Dominic DiTomaso, Avinash Kodi and Ahmed Louri, “QORE: A Fault-Tolerant Network-on-Chip Architecture with Power-Efficient Quad Function Channel (QFC) Buffers,” in Proceedings of the 20th IEEE International Symposium on High-Performance Computer Architecture (HPCA 2014) Orlando, Florida, February 15-19, 2014.
28. Pavan Poluri and Ahmed Louri, “An Improved Router Design for Reliable On-Chip Networks,” in Proceedings, the 28th IEEE International Parallel and Distributed Processing Symposium (IPDPS), Phoenix, Arizona, May 19-23, 2014.
29. Pavan Poluri and Ahmed Louri, “Tackling permanent faults in the Network-on-Chip router pipeline,” in Proceedings of the 25th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), pp. 49-56, Porto de Galinhas, Brazil, October 23-26, 2013.
30. Randy Morris, Avinash Karanth Kodi and Ahmed Louri, “Evaluating the Scalability and Performance of 3D Stacked Reconfigurable Nanophotonic Interconnects,” in proceedings of the 15th IEEE/ACM System Level Interconnect Prediction (SLIP) co-located with Design Automation Conference (DAC), Austin, Texas, June 2, 2013.
31. Randy Morris, Avinash Kodi and Ahmed Louri, “Reconfiguration of 3D Photonic On-chip Interconnects for Maximizing Performance and Improving Fault Tolerance,” in Proceedings of 45th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-45), Vancouver, British Columbia, Canada, Dec 1-5, 2012.
32. Randy Morris, Avinash Kodi and Ahmed Louri, “3D-NoC: 3D Reconfigurable Nanophotonic Interconnects for Multicores,” in Proceedings of 30th IEEE International Conference on Computer Design (ICCD), Montreal, Quebec, Canada, September 30 – October 2, 2012.
33. Dominic DiTomaso, Travis Boraten, Avinash Kodi and Ahmed Louri, “Evaluation of Fault Tolerant Channel Buffers for Improving Reliability in NoCs,” in proceedings of the 55th International Midwest Symposium on Circuits and Systems (MWSCAS), Boise, Idaho, August 5-8, 2012.
34. Jacques Henri Collet, Ahmed Louri, Vivek Tulsidas Bhat, and Pavan Poluri, “ROBUST: a new self-healing fault-tolerant NoC router,” in Proceedings of the 4th International Workshop on Network on Chip Architectures (NoCArc), 2011.
35. A. Kodi, R. Morris, D. DiTomaso, A. Sarathy, and A. Louri, “Co-Design of Channel Buffers and Crossbar Organizations in NoCs Architectures,” in Proceedings of the International Conference on Computer-Aided Design (ICCAD), San Jose, California, November 6-10, 2011.
36. Marcin Janicki, Jacques H. Collet, Ahmed Louri and A. Napieralski, “Hot Spots and Core-to-Core Thermal Coupling in Future Multi-Core Architectures,” in Proceedings of SEMI-THERM, the IEEE 26th Annual Thermal Measurement, Modeling and Management Symposium, Santa Clara, California, February 21-25, 2010.
37. Xiang Zhang and Ahmed Louri, “A Multilayer Nanophotonic Interconnection Network for On Chip Many-core Communications,” in Proceedings of 47th Design Automation Conference (DAC-10), pp. 156-161, Anaheim, California, June 13-18, 2010.
38. J. Sun, R. Lysecky, K. Shankar, A. Kodi, A. Louri and J.M. Wang, “Workload Capacity Considering NBTI Degradation in Multi-Core Systems,” in Proceedings of the 15th Asia and South Pacific Design Automation Conference (ASP-DAC 2010), Taipei, Taiwan, January 18-21, 2010.
39. Ravi Kiran Raghavendra, Avinash Kodi, Ahmed Louri and Janet Wang, "High Speed Inter-Router Link Design for Network-on-Chips (NoC) Architectures,” in Proceedings of the Austin Conference on Integrated Systems and Circuits (ACISC-09), Austin, Texas, October 26-27, 2009.
40. Xiang Zhang and Ahmed Louri, “Nanophotonic Interconnects and 3-D Stacked Technology for Future Many-Core Architectures,” in Proceedings of the Frontiers in Optics 2009, OSA Annual Meeting, San Jose, California, October 12-15, 2009.
41. Avinash Karanth Kodi, Randy Morris, Ahmed Louri and Xiang Zhang, “On-Chip Photonic Network for Scalable Multi-core Architectures,” in Proceedings of the 3rd ACM/IEEE Network- on-Chips (NoCS), San Diego, California, pp. 90, May 10-13, 2009.
42. Avinash Kodi, Ahmed Louri and Janet M. Wang, “Energy-Efficient Router Buffers with By- passing for Network-on-Chips (NoCs),” in Proceedings of the 10th International Symposium on Quality Electronic Design (ISQED'09), San Jose, California, March 16-18, 2009.
43. Sun Jin, Avinash Kodi, Ahmed Louri and Janet M. Wang, “NBTI Aware Workload Balancing in Multi-core Systems,” in Proceedings of the 10th International Symposium on Quality Electronic Design (ISQED'09), San Jose, California, March 16-18, 2009.
44. Avinash Karanth Kodi, Ashwini Sarathy, Ahmed Louri and Janet M. Wang, “Adaptive Inter-router Links for Low-Power, Area-Efficient and Reliable Network-on-Chip (NoC) Architectures,” in Proceedings of the 14th Asia and South Pacific Design Automation Conference (ASP-DAC'09), Yokohama, Japan, January 19-22, 2009.
45. Avinash Kodi and Ahmed Louri, “Efficient Dynamic Bandwidth Re-allocation in Photonic Networks using SOI-based Microring Resonators,” in Proceedings of Frontiers in Optics, OSA Annual Meeting, Rochester, New York, October 19- 23, 2008.
46. Avinash Kodi, Ashwini Sarathy, and Ahmed Louri, “iDEAL: Inter-router Dual-function Energy- and Area-Efficient Link design for Network-on-Chip (NoC) Architecture,” in Proceedings of the International Symposium on Computer Architecture (ISCA-35), Beijing, China, pp. 241-250, June 21-25, 2008.
47. Avinash Kodi, Ashwini Sarathy, and Ahmed Louri, “Design of Adaptive Communication Channel Buffers for Low-Power Area-Efficient Network-on-Chip Architecture,” in Proceedings of the ACM/IEEE Symposium on Architectures for Networking and Communications Systems, (ANCS 2007), pp. 4 -56, Orlando, Florida, December 3-4, 2007.
48. Avinash Kodi and Ahmed Louri, “Performance Adaptive Power-Aware Reconfigurable Optical Interconnects for High-Performance Computing Systems,” in Proceedings of the International Conference for High-Performance Computing, Networking, Storage and Analysis, (SC' 07), Reno, Nevada, November 10-16, 2007.
49. Chander Kochar, Avinash Karanth Kodi and Ahmed Louri, “Implementation of Dynamic Band- width Re-allocation in Optical Interconnects using Micro-ring Resonators,” in Proceedings of 15th Annual IEEE Symposium on High-Performance Interconnects (Hot Interconnects), Stanford, California, August 22-24, 2007.
50. Avinash Karanth Kodi, and Ahmed Louri, “Power-Aware Bandwidth Reconfigurable Optical Interconnects for High-Performance Computing (HPC) Systems,” in Proceedings of the 22nd IEEE International Parallel and Distributed Processing Symposium, (IPDPS'07), Long Beach, California, March 26-30, 2007.
51. Avinash Karanth Kodi and Ahmed Louri, “A New Technique for Dynamic Bandwidth Reallocation in Optically Interconnected High-Performance Computing Systems,” in Proceedings of the 14th Annual IEEE Symposium on High-Performance Interconnects, (Hoti14), Stanford, August 23-25, 2006.
52. Avinash Karanth Kodi and Ahmed Louri, “Switchless Photonic Architecture for Parallel Computers,” in Proceedings of Frontiers in Optics, 89th OSA Annual Meeting, Tucson, Arizona, October 16-20, 2005.
53. Avinash Karanth Kodi and Ahmed Louri, “Scalable Optical Interconnection Network for Parallel and Distributed Computing,” in Proceedings of Information Photonics, Optical Society of America, Charlotte, North Carolina, June 6-9, 2005.
54. Avinash Karanth Kodi and Ahmed Louri, “Design of a High-Speed Optical Interconnect for Scalable Shared Memory Multiprocessors,” in Proceedings of the 12th Annual IEEE Symposium on High Performance Interconnects (Hot Interconnects), Stanford, California, August 25-27, 2004.
55. Avinash Karanth Kodi and Ahmed Louri, “A Scalable Architecture for Distributed Shared Memory Multiprocessors using Optical Interconnects,” in Proceedings of 18th International Parallel and Distributed Processing Symposium (IPDPS'04), Santa Fe, New Mexico, April 26-30, 2004.
56. Ahmed Louri and Avinash Karanth Kodi, “Parallel Optical Interconnection Network for SMPs,” in Proceedings of Frontiers in Optics, 87th OSA Annual Meeting, Tucson, Arizona, October 5-9, 2003.
57. Ahmed Louri and Avinash Karanth Kodi, “Design of Large-scale Symmetric Multiprocessors (SMPs) using Parallel Optical Interconnects,” in Proceedings of the ACS/IEEE International Conference on Computer Systems and Applications, AICCSA '03, Tunis, Tunisia, July 14-18, 2003.
58. Avinash Kodi and Ahmed Louri, “Optical Interconnects for Large-Scale Symmetric Multiprocessor Networks,” in Proceedings of the OSA/IEEE Optics in Computing 2002, Taipei, Taiwan, April 2002.
59. Peng Yin Choo and Ahmed Louri, “A DWDM IP-Routing Lookups and Forwarding Scheme using Multiwavelength Optical Content-addressable Memory Processing,” in Proceedings of the Sixth International Conference on Computer Science and Informatics, Durham, North Carolina, March 8-16, 2002.
60. Avinash Kodi and Ahmed Louri, “Y-junction Based addressing in Optical Symmetric Multiprocessor Networks,” in Proceedings of the International Annual Meeting of the Lasers and Electro-Optics Society, LEOS 2001, pp. 68-72, San Diego, California, November 11-15, 2001.
61. Russ Ivey and Ahmed Louri, “Optical Crossbar-Connected Networks for Scalable Parallel Computing Systems,” in Proceedings of the International OSA/IEEE Topical Meeting on Optics in Computing 2001, Lake Tahoe, Nevada, January 9-11, 2001.
62. Peng Yin Choo and Ahmed Louri, “Guide-wave Multiwavelength Processing Module for Networking Applications,” in Proceedings of the International OSA/IEEE Topical Meeting on Optics in Computing 2001, Lake Tahoe, Nevada, January 9-11, 2001.
63. Russ Ivey and Ahmed Louri, “Crossbar-Connected Optical Interconnects using VCSEL Arrays,” in Proceedings of the OSA Annual Meeting, Optics for the New Millennium, Providence, Rhode Island, October 2 -26, 2000.
64. Peng Yin Choo and Ahmed Louri, “Guided-wave Multiwavelength Computing Systems,” in Proceedings of the OSA Annual Meeting, Optics for the New Millennium, Providence, Rhode Island, October 22-26, 2000.
65. Peng Yin Choo and Ahmed Louri, “The Equivalency Processing Parallel Photonic Integrated Circuit (EPI3C): A Parallel Digital Equivalence and Fussy Search Module,” in Proceedings of the Applied Imagery Pattern Recognition Annual Workshop, Imagery in the New Millennium, Washington, D.C., October 16-18, 2000.
66. Brian Webb and Ahmed Louri, “Compact WDM VCSEL-Based Optical Crossbar for High-Density Chip-to-Chip and Board-to-Board Interconnects,” in Proceedings of the Symposium on Hot Interconnects'7, pp. 17 -180, Stanford, California, August 18-20, 1999.
67. Peng Yin Choo, Abram Detofsky and Ahmed Louri, “A Multi-Wavelength Optical Content- Addressable Parallel Processor (MW-OCAPP) for High-Speed Parallel Relational Database Processing: Architectural Concepts,” in Proceedings of the International OSA/IEEE Topical Meeting on Optics in Computing'99, pp. 66-69, Snowmass, Colorado, April 12-16, 1999.
68. Peng Yin Choo, Abram Detofsky and Ahmed Louri, “A Multi-Wavelength Optical Content- Addressable Parallel Processor for High-Speed Parallel Relational Database Processing: Experimental System,” in Proceedings of the IEEE International Workshop on Optics in Computer Science (WOCS'99), pp. 873-887, San Juan, Puerto Rico, April 14-16, 1999.
69. Thomas Jones and Ahmed Louri, “Media Access Protocols for a Scalable Optical Interconnection Network,” in Proceedings of the International Conference on Parallel Processing (ICPP), Minneapolis, Minnesota, August 15-20, 1998.
70. Thomas Jones and Ahmed Louri, “Channel Allocation, Power Budget and Bit Error Rate in Hierarchical Optical Ring Interconnection Network (HORN),” in Proceedings of the IEEE/OSA International Conference on Massively Parallel Processing using Optical Interconnections (MPPOI'98), pp. 123-130, Las Vegas, Nevada, June 14-16, 1998.
71. Brian Webb and Ahmed Louri, “A Free-Space Optical Crossbar Switch using Wavelength Division Multiplexing and Vertical Cavity Surface Emitting Lasers,” in Proceedings of the IEEE/OSA International Conference on Massively Parallel Processing Using Optical Interconnections (MPPOI'98), pp. 50-57, Las Vegas, Nevada, June 14-16, 1998.
72. Peng Yin Choo, Abram Detofsky and Ahmed Louri, “An Optical Architecture Based on Multiwavelength and Polarization for Parallel and High-Speed Relational Database Processing,” in Proceedings of the OSA/IEEE Optics in Computing (OC'98), SPIE Vol. 3490, pp. 139-143, Brugge, Belgium, June 17-20, 1998.
73. Ahmed Louri and Rajdeep Gupta, “Hierarchical Optical Ring Interconnection: A WDM-Based Scalable Network for Multiprocessing and Multicomputing,” in Proceedings of the IEEE/OSA International Conference on Massively Parallel Processing using Optical Interconnections (MPPOI'96), pp. 247 - 255, Maui, Hawaii, October 27 - 29, 1996.
74. Ahmed Louri and Hongki Sung, “An Efficient 3-D Implementation of Binary De Bruijn Networks with Applications to Massively Parallel Computing,” in Proceedings of the IEEE/OSA International Conference on Massively Parallel Processing using Optical Interconnections (MPPOI'95), pp. 152 - 159, San Antonio, Texas, October 23 - 24, 1995.
75. Ahmed Louri, James Hatch and Jonwhoa Na, “A Novel Constant-Time Parallel Sorting Algorithm and its Optical Implementation using Smart Pixels,” in Proceedings of the OSA/IEEE Annual Topical Meeting on Optical Computing, Salt Lake City, Utah, March 12 - 17, 1995.
76. Ahmed Louri, Hongki Sung, Yookeon Moon, and Bernard P. Zeigler, “An Efficient Signal Distinction Scheme for Large-Scale Free-Space Optical Networks Using Genetic Algorithms,” in Proceedings of the OSA/IEEE Annual Topical Meeting on Photonics in Switching, Salt Lake City, Utah, March 12 - 17, 1995.
77. Ahmed Louri and Hongki Sung, “Free-Space Optical Implementation of DeBruijn Networks,” in Proceedings of the Annual Meeting of The Optical Society of America, Dallas, Texas, October 2 - 7, 1994.
78. Ahmed Louri and Hongki Sung, “A Scalable Optical Interconnection Network for Massively Parallel Computers,” in Proceedings of the OSA/IEEE International Conference on Optical Computing, Edinburgh, Scotland, August 22-25, 1994.
79. Ahmed Louri and James Hatch Jr., “The Physical Design of an Optical Content-Addressable Parallel Processor,” in Proceedings of the OSA/IEEE International Conference on Optical Computing, Edinburgh, Scotland, August 22-25, 1994.
80. Ahmed Louri and James Hatch Jr., “An Optical Content-Addressable Parallel Processor for High- Speed Database Processing,” in Proceedings of the Frontiers in Information Optics, Topical Meeting of the International Commission for Optics, Kyoto, Japan, April 4 - 8, 1994.
81. Ahmed Louri and Hongki Sung, “A Hypercube-Based Optical Interconnection Network: A Solution to the Scalability Requirements for Massively Parallel Computing,” in Proceedings of the IEEE/OSA International Workshop on Massively Parallel Processing Using Optical Interconnections (MPPOI'94), pp. 8 -93, Cancun, Mexico, April 26-27, 1994.
82. Ahmed Louri and Earl Hokens, “Performance Considerations Relating to the Design of Interconnection Networks for Multiprocessing Systems,” in Proceedings of the International Conference on Parallel Processing (ICPP), St. Charles, Illinois, August 1993.
83. Ahmed Louri and Hongki Sung, “Efficient Implementation Methodology for 2-D Space-Invariant Hypercube-Based Free-Space Optical Interconnection Networks,” in Proceedings of the OSA/IEEE International Topical Meeting on Photonics in Switching, Palm Springs, California, March 15-17, 1993.
84. Ahmed Louri and James Hatch, “High-Speed Database Processing on an Optical Content- Addressable Parallel Processor (OCAPP),” in Proceedings of the OSA/IEEE International Topical Meeting on Optical Computing, Palm Springs, California, March 16-19, 1993.
85. Ahmed Louri, “An Algorithm for Implementing Fully-Connected Optical Interconnection Networks with Broadcast Capability,” in Proceedings of the OSA/IEEE International Topical Meeting on Optical Computing, Palm Springs, California, March 16-19, 1993.
86. Ahmed Louri and Hongki Sung, “A Compiler Directed Cache Coherence Scheme with Fast and Parallel Explicit Invalidation,” in Proceedings of the International Conference on Parallel Processing (ICPP), St. Charles, Illinois, August 17-21, 1992.
87. Ahmed Louri and Hongki Sung, “A New Compiler-Directed Cache Coherence Scheme for Shared Memory Multiprocessors with Fast and Parallel Explicit Invalidation,” in Proceedings of the 19th Annual International Symposium on Computer Architecture (ISCA), Queensland, Australia, May 19-23, 1992.
88. Ahmed Louri and J. Na, “An Optical Inference Engine for Fast and Parallel Execution of Rule Based Systems,” in Proceedings of the 19th Annual International Symposium on Computer Architecture (ISCA), Queensland, Australia, May 19-23, 1992.
89. Ahmed Louri and J. Na, “Parallel Optical Rule-Based Systems for Fast Execution of Expert Systems,” in Proceedings of the 25th Hawaii International Conference on Systems Sciences, Kona, Hawaii, January 1992.
90. Ahmed Louri and H. Lee, “Microcanonical Mean Field Annealing: A New Algorithm for Increasing the Convergence Speed of Annealed Neural Networks,” in Proceedings of the Joint Conference on Neural Networks, Singapore, November 1991.
91. Ahmed Louri, S.Y. Kuo, and S. C. Liang, “Design and Evaluation of Fault-Tolerant Interleaved Memory Systems,” in Proceedings of the 20th Annual International Conference on Parallel Processing, Chicago, Illinois, August 1991.
92. Ahmed Louri, “An Optical Content-Addressable Parallel Architecture for Fast Searching and Retrieving,” in Proceedings of the Parallel Architectures and Languages Europe (PARLE' 91), Eindhoven, Netherlands, June 1991.
93. Ahmed Louri, “Design of Optical Associative Parallel Processors with Applications to Fast Searching and Information Retrieval,” in Proceedings of the Fifth International Parallel Processing Symposium (IPPS), Fullerton, California, April 1991.
94. Ahmed Louri, “Roles of Optics in High-Performance Computing Systems,” in Proceedings of the First Workshop on Architectures for Free Space Digital Optical Computing and Networking, Vail, Colorado, January 1991.
95. Ahmed Louri and Arthur Post, “Optimal Implementation of Arbitrary Boolean Functions using Space-Variant Optics,” in Proceedings of OPTCON' 90, Boston, Massachusetts, November 1990.
96. Ahmed Louri, “Parallel Implementation of Multi-Rule Optical Symbolic Substitution Processors Using Wavelength Multiplexing,” in Proceedings of the OSA/IEEE International Topical Meeting on Optical Computing, Kobe, Japan, April 1990.
97. Ahmed Louri, “Impact of Data Encoding Schemes on the Throughput of Optical Symbolic Substitution Systems,” in Proceedings of the OSA/IEEE International Topical Meeting on Optical Computing, Kobe, Japan, April 1990.
98. Ahmed Louri, “Symbolic Substitution-Based Optical Architectures and Algorithms for High-Speed Parallel Processing,” in Proceedings of the ACM 1990 Computer Science Conference, February 1990.
99. Ahmed Louri, “A Preliminary Version of an Optical Data-Flow Multiprocessing System,” in Proceedings of the Hawaii Int'l Conference on System Science-23, pp. 121-130, Kona, Hawaii, January 3-6, 1990.
100. Ahmed Louri, “An Optical Architecture and Algorithms for Data-Parallel Computing,” in Proceedings of the Thirteenth Annual Computer Software and Applications Conference, Orlando, Florida, September 18-22, 1989.
101. Ahmed Louri, “An Optical Data-Flow Computer,” in Proceedings of the 33rd Annual International Symposium on Optical and Electro-Optical Applied Science and Engineering, Conference on Optical Information Processing Systems and Architectures, pp.47-60, San Diego, California, August 6- 11, 1989.
102. Ahmed Louri, “A Massively Parallel Optical Computer,” in Proceedings of the OSA/IEEE Topical Meeting on Optical Computing, Vol. 9, pp.96-100, Salt Lake City, Utah, February 1989.
103. Kai Hwang and Ahmed Louri, “Optical Arithmetic Using Symbolic Signed-Digit Substitution,” in Proceedings of the 17th International Conference on Parallel Processing, pp. 55-65, St. Charles, Illinois, August 15-19, 1988.
104. Ahmed Louri and Kai Hwang, “A Bit-Plane Architecture for Optical Computing with 2-D Symbolic Substitution,” in Proceedings of the 15th Annual International Symposium on Computer Architecture (ISCA), pp. 18-30, Honolulu, Hawaii, May 30-June 2, 1988.
105. Kai Hwang and Ahmed Louri, “New Symbolic Substitution Algorithms for Optical Arithmetic using Signed-Digit Representation,” in Proceedings of the Soc. Photo-Opt. Instr. Eng. (SPIE), Vol. 880, pp. 90-100, Los Angeles, California, January 1988.
106. Ahmed Louri and Kai Hwang, “Parallel Architectures for Optical Computing,” in Proceedings of the Third International SIAM Conference on Parallel Processing and Scientific Computing, pp. 414-428, Los Angeles, California, December 1-4, 1987.
107. Ahmed Louri and Kai Hwang, “Ultrafast Optical Arithmetic Architecture with Symbolic Substitution,” in Proceedings of Optics '87, 1987 Annual OSA Meeting, Rochester, New York, October 18-23, abstract also published in Optics News, Vol. 13, No. 19, pp. 126-127, September 1987.
108. Kai Hwang, Zhiwei Xu and Ahmed Louri, “Remps: An Electro-Optical Supercomputer for Parallel Solution of PDE Problems,” in Proceedings of the 2nd International Conference on Supercomputing, pp. 301-311, Santa Clara, California, May 5-8, 1987.

**Active Grants (2020)**

* “Neural-Network-based Stochastic Computing Architectures with applications to Machine Learning,” National Science Foundation.
* “Photonic Neural Network Accelerators for Energy-efficient Heterogeneous Multicore Architectures,” National Science Foundation.
* “Integrated Framework for System-Level Approximate Computing,” National Science Foundation.
* “Machine-Learning Enabled Network-on-Chip Architectures Optimized for Power, Performance and Reliability,” National Science Foundation.
* “SPARTA: a Stream-based Processor and Run-Time Architecture,” National Science Foundation.
* “A Holistic Design Methodology for Fault-Tolerant and Robust Network- on-Chips (NoCs) Architectures,” National Science Foundation.
* “Scaling On-chip Networks to 1000-core Systems using Heterogeneous Emerging Interconnect Technologies,” National Science Foundation.
* “Power-Efficient and Reliable 3D Stacked Reconfigurable Photonic Network-on-Chips for Scalable Multicore Architectures,” National Science Foundation.
* David and Marilyn Karlgaard Endowment Fund

**Patents (2020)**

USPTO Full Patent filed:

1. No. 10,148,593 “Directional Allocation of Communication Links based on Data Traffic Loads”.
2. No. UA 08-078, “Inter-Router Dual-Function Energy and Area-Efficient Links for Network-on-Chips".
3. No. UA 08-081 “Fault-and Variation Tolerant Energy-and Area-Efficient Links for Network-on-Chips".
4. No.16/547,161, “EZ-Pass and Energy-Efficient and High-Performance Router Architecture for Scalable Network-on-Chips”.
5. No. 16/547,297, “Reinforcement Learning for Fault-tolerant, Energy-efficient NoC Design”.

USPTO Provisional Patent filed:

1. No. 63/019,720, "Learning-Based High-Performance, Energy-Efficient, and Secure Interconnection Design Framework”.
2. No. 63/019,670, "A Versatile and Flexible Interconnection Network Design for Chiplet-Based Manycore Architecture”.
3. No. 63/019,752, “Approximate Communication Framework for Network-on-Chips”.
4. No. 62/853,418, “A Learning-Enabled Energy-Efficient On-Chip Interconnection".
5. No. 62/853,455, "A Machine Learning-Based, High-Performance, Energy-Efficient, and Reliable Network-on-Chip Design”.